Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1-19. (Canceled)

20. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer including a source region on an insulating surface;

a gate insulating film on and in contact with the semiconductor layer, the gate insulating film defining a contact hole extending from a first opening located at a top surface of the gate insulating film to a second opening located at a bottom surface of the gate insulating film, and the semiconductor layer defining a recess having a third opening located in a top surface of the source region that is in communication with the second opening, the third opening defining an area that is greater than an area defined by the second opening such that a portion of the gate insulating film extends directly over a portion of the recess;

a gate electrode on the gate insulating film; and

a source electrode in contact with the semiconductor layer through the contact hole,

wherein the source electrode contains a first layer and a second layer,

wherein the recess is filled with the first layer,

wherein the first layer is in contact with the gate insulating film,

wherein the first layer is an alloy of aluminum and an element belonging to one of groups 12 to 15, [[and]]

wherein the element belonging to one of groups 12 to 15 is at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony, and

wherein the contact hole is directly over the source region.

21-27. (Canceled)

28. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the semiconductor layer contains crystalline silicon.

29. (Canceled)

30. (Canceled)

31. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the second layer contains aluminum.

32. (Canceled)

33. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the semiconductor device is an active matrix type EL display device.

34. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer including a source region on an insulating surface;

a gate insulating film on and in contact with the semiconductor layer, the gate insulating film defining a first contact hole extending from a first opening located at a top surface of the gate insulating film to a second opening located at a bottom surface of the gate insulating film, and the semiconductor layer defining a first recess having a third opening located in a top surface of the source region that is in communication with the second opening, the third opening defining an area that is greater than an area defined by the second opening such that a portion of the gate insulating film extends directly over a portion of the first recess;

a gate electrode on the gate insulating film;

an anodic oxide film on the gate electrode;

an interlayer insulating film on and in contact with the anodic oxide film, the interlayer insulating film defining a second contact hole extending from a fourth opening located at a top surface of the interlayer insulating film to a fifth opening located at a bottom surface of the interlayer insulating film, and the anodic oxide film defining a second recess having a sixth opening located at a top surface of the anodic oxide film that is in communication with the fifth opening, the sixth opening defining an area that is greater than an area defined by the fifth opening such that a portion of the interlayer insulating film extends directly over a portion of the second recess; and

a source electrode in contact with the semiconductor layer through the first contact hole and a wiring in contact with the gate electrode through the second contact hole,

wherein the source electrode contains a first layer and a second layer,

wherein the wiring contains a third layer and a fourth layer,

wherein the first recess is filled with the first layer,

wherein the second recess is filled with the third layer,

wherein the first layer is in contact with the gate insulating film,

wherein the first layer is an alloy of aluminum and an element belonging to one of groups 12 to 15, [[and]]

wherein the element belonging to one of groups 12 to 15 is at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony, and

wherein the first contact hole is directly over the source region.

35. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the semiconductor layer contains crystalline silicon.

36. (Canceled)

37. (Canceled)

38. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the second layer contains aluminum.

39. (Canceled)

40. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the semiconductor device is an active matrix type EL display device.

41. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer including a source region on an insulating surface, wherein the semiconductor layer has a side recess in the source region;

a gate insulating film on the semiconductor layer;

a gate electrode on the gate insulating film;

an interlayer insulating film over at least the gate electrode; and

a source electrode over the interlayer insulating film,

wherein the source electrode is in contact with the semiconductor layer through a contact hole that is opened in the interlayer insulating film and the gate insulating film, ~~and that is directly over the source region,~~

wherein the contact hole is directly over the source region,

wherein the source electrode contains a first layer and a second layer,

wherein a part of the first layer and a part of the second layer are located directly over the interlayer insulating film,

wherein the side recess is filled with the first layer,

wherein the first layer is in contact with the gate insulating film,

wherein the first layer is an alloy of aluminum and an element belonging to one of groups 12 to 15, and

wherein the element belonging to one of groups 12 to 15 is at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

42. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the semiconductor layer contains crystalline silicon.

43. (Canceled)

44. (Canceled)

45. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the second layer contains aluminum.

46. (Canceled)

47. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the interlayer insulating film contains at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

48. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the semiconductor device is an active matrix type EL display device.

49. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer including a source region on an insulating surface, wherein the semiconductor layer has a first side recess in the source region;

a gate insulating film on the semiconductor layer;

a gate electrode on the gate insulating film, wherein the gate electrode has a second side recess;

an interlayer insulating film over at least the gate electrode; and

a source electrode and a wiring over the interlayer insulating film,

wherein the source electrode is in contact with the semiconductor layer through a first contact hole that is opened in the interlayer insulating film and the gate insulating film, ~~and that is directly over the source region, and~~

wherein the first contact hole is directly over the source region,

wherein the wiring is in contact with the gate electrode through a second contact hole opened in the interlayer insulating film,

wherein the source electrode contains a first layer and a second layer and the wiring contains a third layer and a fourth layer,

wherein a part of the first layer, a part of the second layer, a part of the third layer and a part of the fourth layer are located directly over the interlayer insulating film,

wherein the first side recess is filled with the first layer,

wherein the second side recess is filled with the third layer,

wherein the first layer is in contact with the gate insulating film,

wherein the first layer is an alloy of aluminum and an element belonging to one of groups 12 to 15, and

wherein the element belonging to one of groups 12 to 15 is at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

50. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the semiconductor layer contains crystalline silicon.

51. (Canceled)

52. (Canceled)

53. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the second layer contains aluminum.

54. (Canceled)

55. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the interlayer insulating film contains at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

56. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the semiconductor device is an active matrix type EL display device.

57. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the first layer is flowable at less than 450 °C.

58. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the first layer is flowable at less than 450 °C.

59. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the first layer is flowable at less than 450 °C.

60. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the first layer is flowable at less than 450 °C.